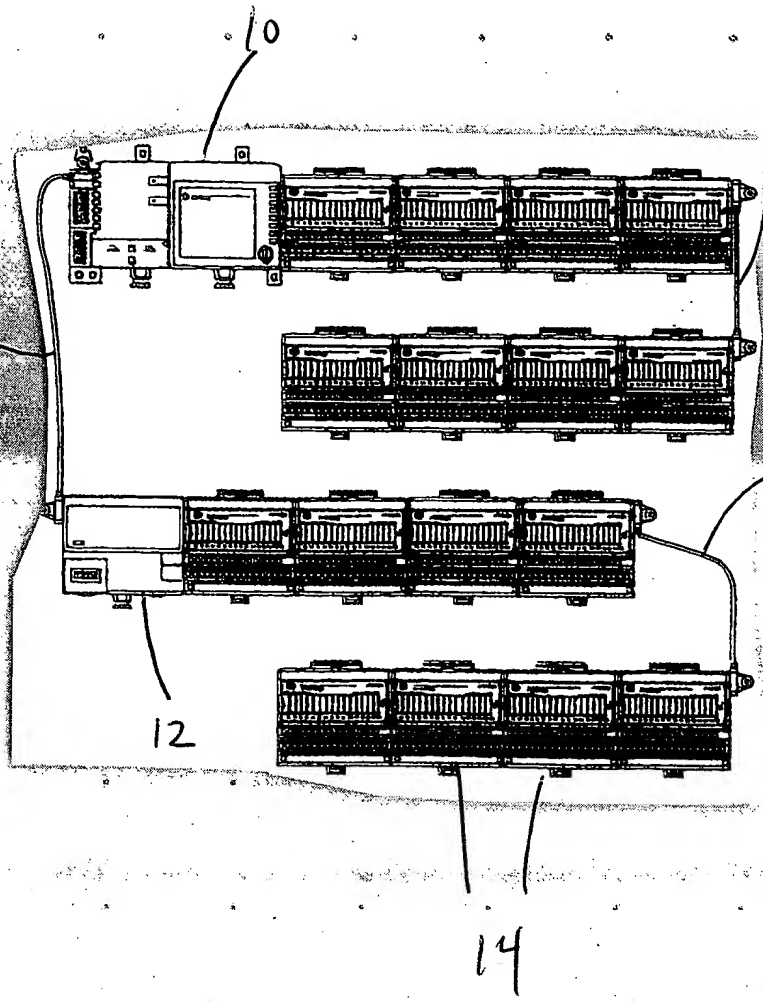


Fig. 1

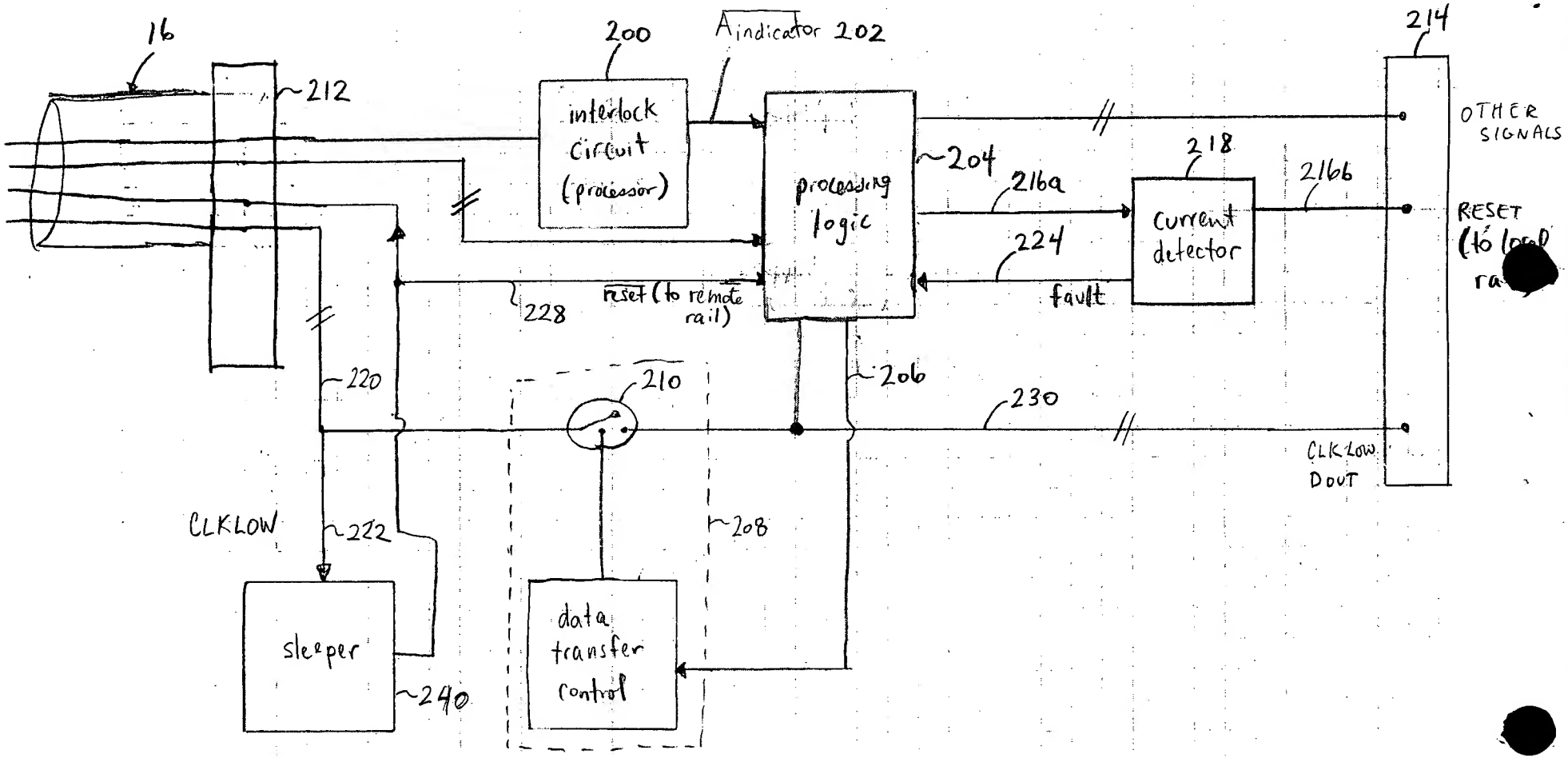

16
212
200
interlock circuit (processor)
A indicator 202
processing logic
204
214
OTHER SIGNALS
218
current detector
216a
216b
RESET (to load
224
fault
reset (to remote rail)
228
220
210
206
230
CLK LOW
DOUT
CLKLOW
222
208
sleeper
240
data transfer control

Fig. 2

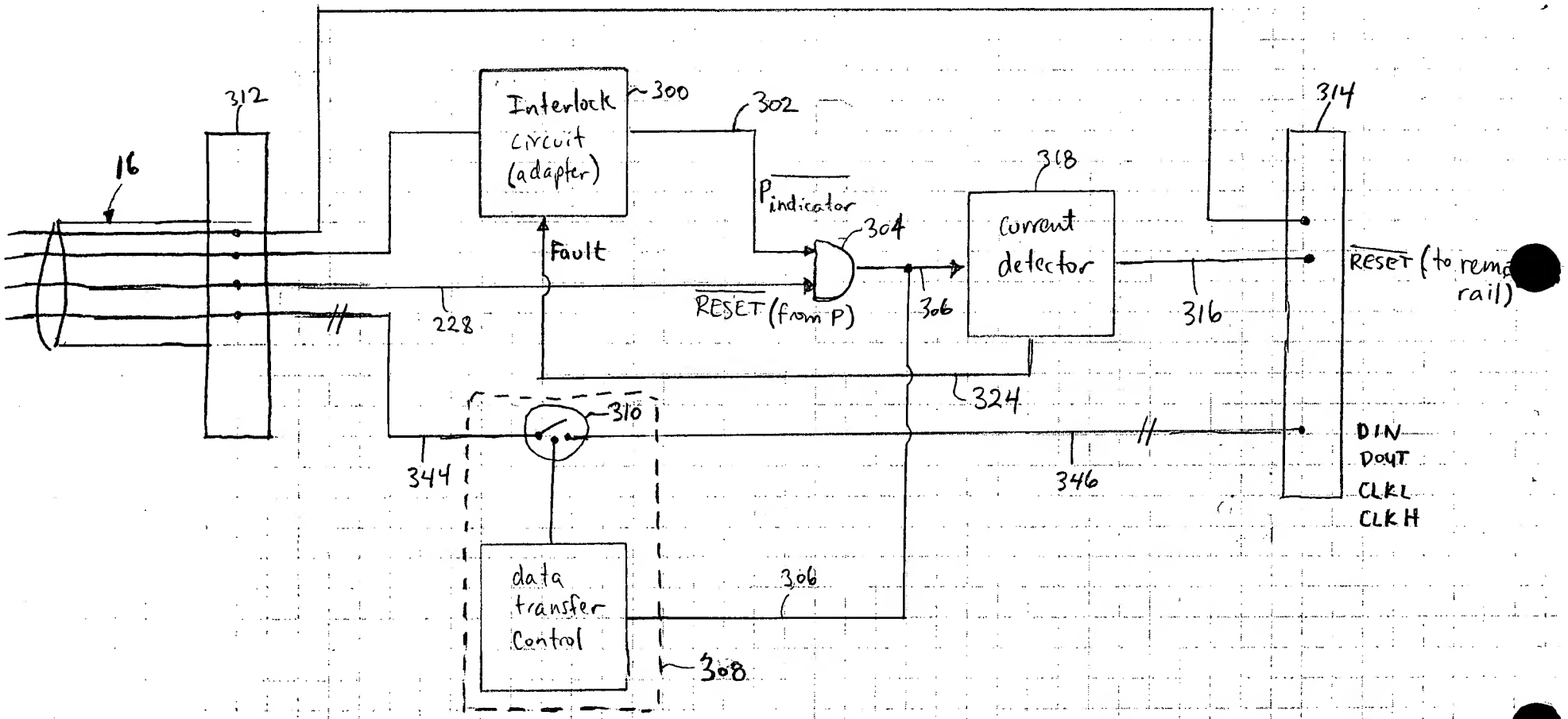
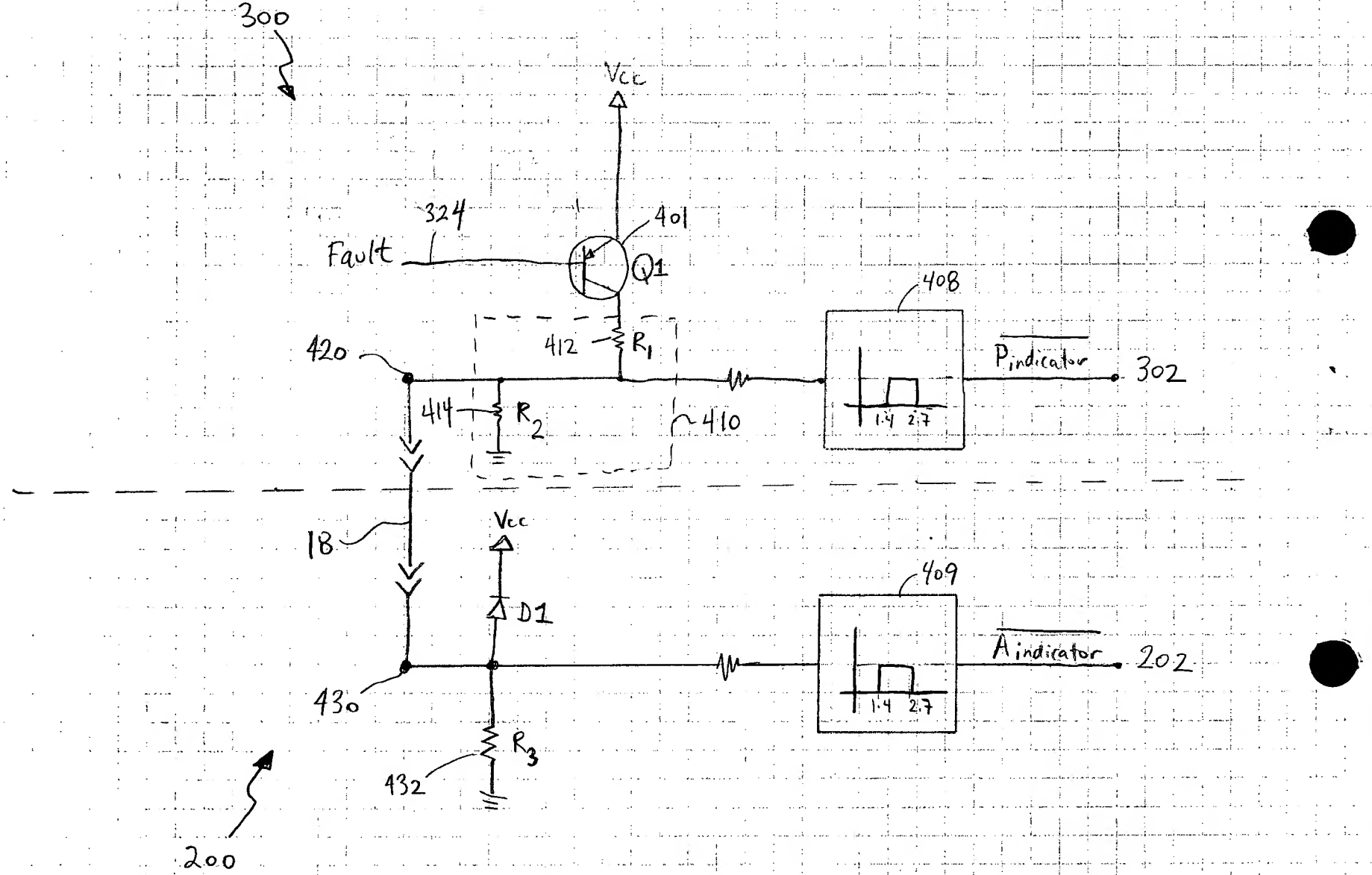

16
312
Interlock circuit (adapter)
300
302
314
318
$\overline{P_{indicator}}$
304
Current detector
Fault
$\overline{RESET}$ (from P)
$\overline{RESET}$ (to rema rail)
228
306
316
324
310
344
346
DIN
DOUT
CLKL
CLKH
data transfer Control
306
308

Fig-3

Fig. 4



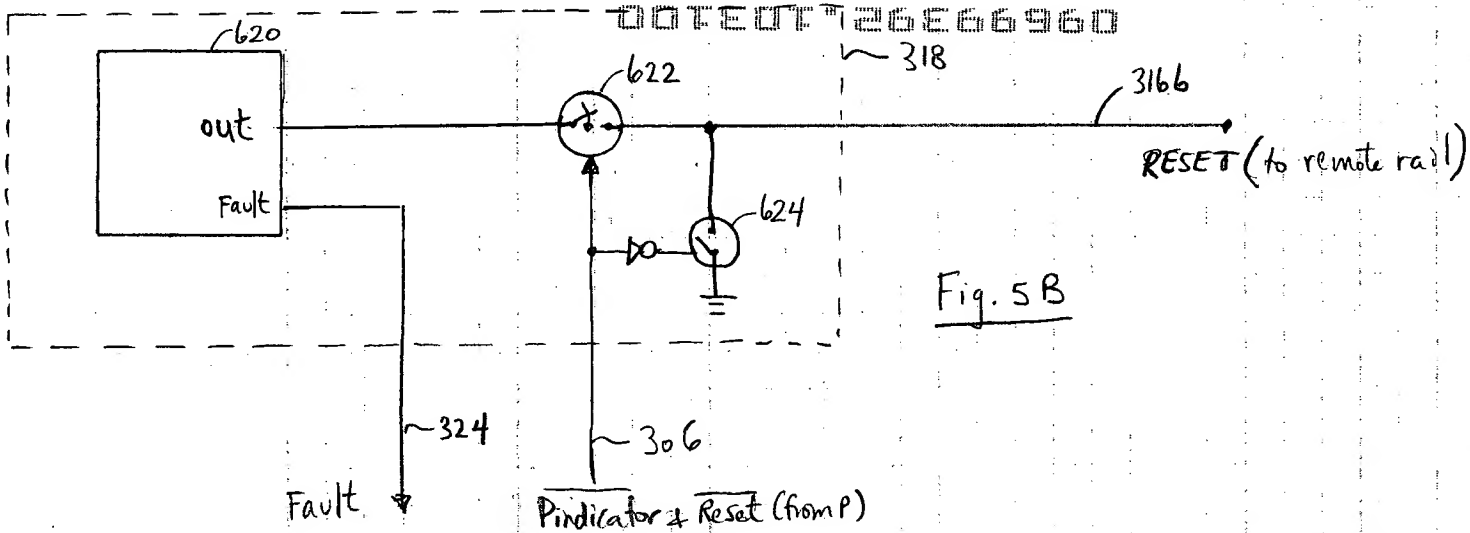

620
out
Fault
622
624
318
3166
RESET (to remote rail)
324
306
Fault
Pindicator + Reset (from P)

Fig. 5B

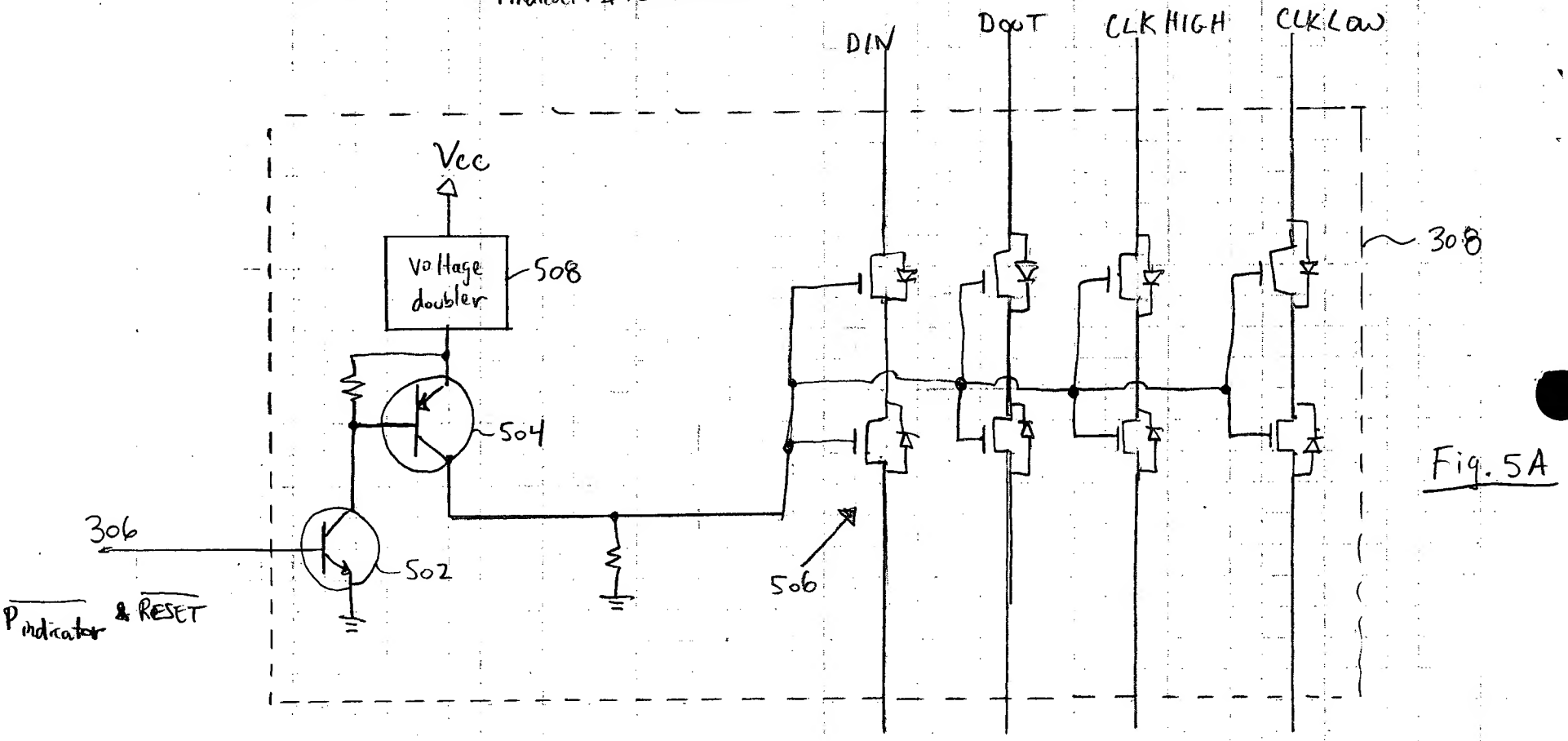

DIN
DOUT
CLK HIGH
CLK Low
Vcc
Voltage doubler
508
504
502
306
506
308
Pindicator & RESET

Fig. 5A

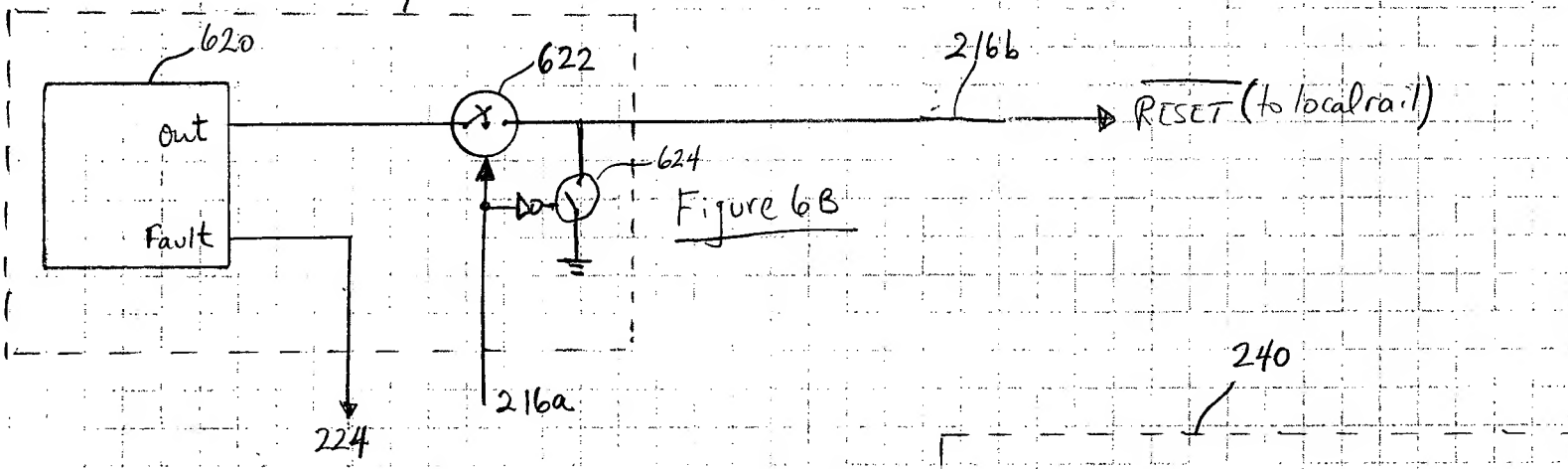


Figure 6B

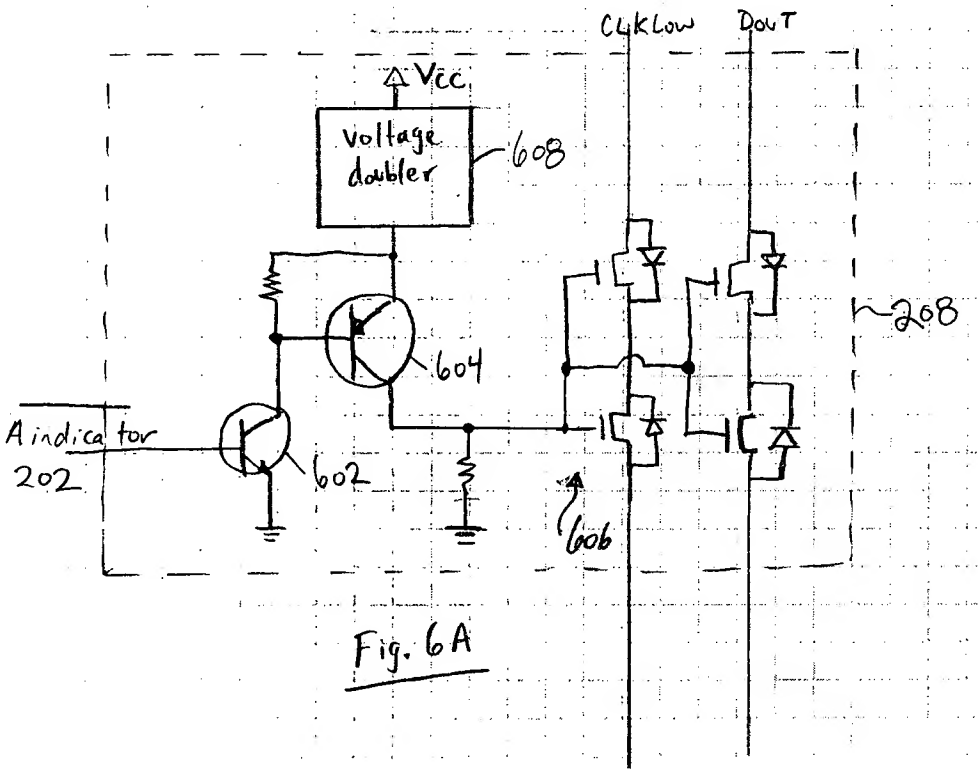


Fig. 6A

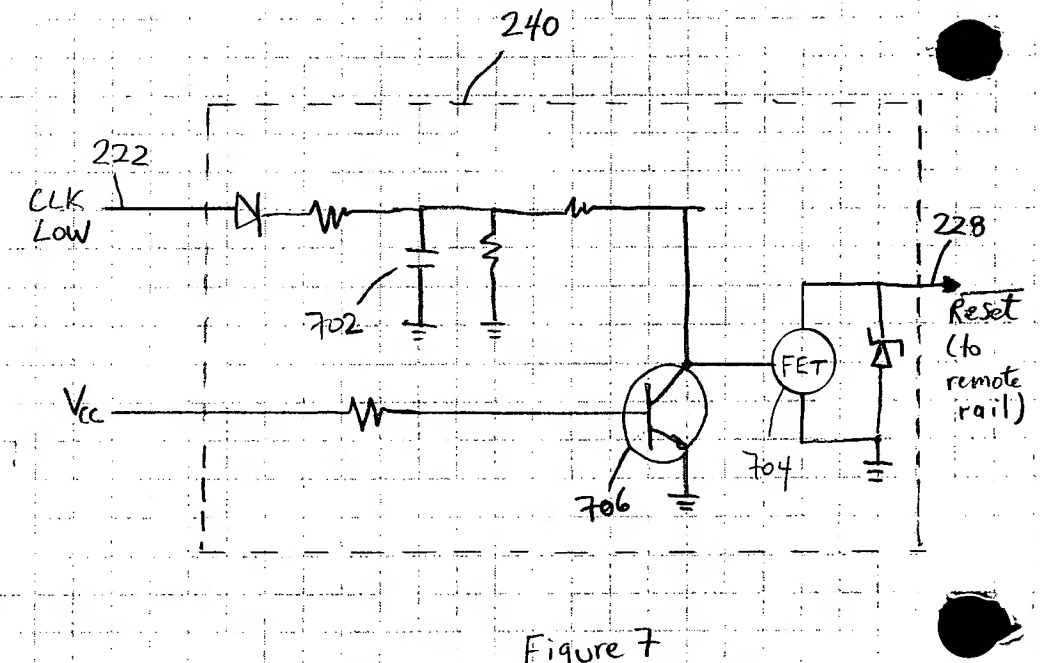


Figure 7

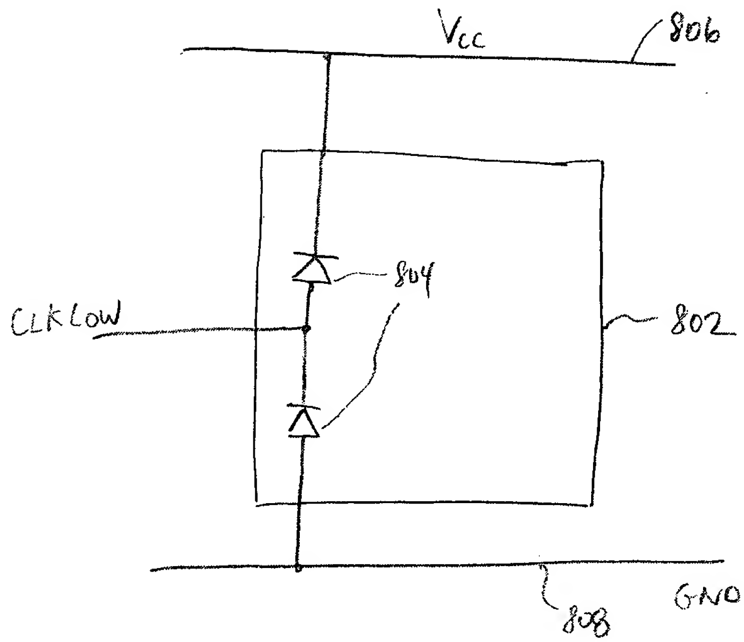


Fig. 8